REMARKS

Reconsideration of this application, as presently amended, is respectfully requested. Claims 1-20 are pending in this application. Claims 16 and 20 stand rejected. Claims 1-12 are withdrawn from consideration as being directed to a non-elected invention. Claims 13-15 and 17-19 are apparently allowable. More specifically, on page 5, lines 4-6 of the final Office Action, the Examiner indicates that "claims 13-15 and 17-19 would be allowable if rewritten to overcome the objections set forth in this Office Action." However, there are no objections to any of claims 13-15 and 17-19. Therefore, claims 13-15 and 17-19 should be in condition for allowance.

Applicants would like to thank the Examiner for the courtesies extended to applicant's representative during the personal interview with the Examiner conducted on July 25, 2006. During the course of the interview, the final rejection of claims 16 and 20 in view of the cited prior art (i.e., Fig. 16 of the applicant's application) was discussed. In particular, applicant's representative argued that the cited prior art does not disclose the claimed "arithmetic circuit" recited in claims 16 and 20. In response to the patentability arguments presented during the interview, the Examiner discussed how the claim language is being interpreted to correspond to the claimed "arithmetic circuit".

Although no agreement was reached, in view of the discussions during the interview and in order to expedite prosecution, claims 16 and 20 have been amended, as will be discussed below, to clarify the invention.

Claim Rejections – 35 U.S.C. §102

In the final Office Action mailed March 8, 2006, claims 16 and 20 were rejected under 35 U.S.C. §102(a) as being anticipated by Applicant's admitted prior art (**AAPA**) Fig. 16. This rejection, to the extent it is considered to apply to the present claims, is respectfully traversed.

Claims 16 and 20 have been amended to recite that the claimed "logic circuit" ***produces a matrix*** and the claimed "arithmetic circuit" multiplies the predetermined initial values by the ***matrix produced by the logic circuit***. Support for this amendment is provided, e.g., in Fig. 13, wherein the elements 27, 28a, 28b and 28c are considered "logic circuit" that produces a matrix Mo, and the element 28d is considered an "arithmetic circuit" that multiplies the matrix Mo by predetermined initial values Ri stored in a storage circuit 22.

In contrast to the claimed invention, as seen in Fig. 16, the matrices ***produced*** by the logic circuit are **not** used by the arithmetic circuit for multiplication with the predetermined initial values Ri. More specifically, as shown in Fig. 16, the arithmetic circuit 21 multiplies predetermined initial values $Ri = Ri_3\text{-}Ri_0$ stored in initial value buffer 22 by matrices $M_{3(100)}$, $M_{2(100)}$, $M_{1(100)}$, $M_{0(100)}$ that are obtained and stored in advance (see page 9, lines 7-9 of Applicant's specification). However, the predetermined initial values $Ri = Ri_3\text{-}Ri_0$ are **not** multiplied by a matrix produced by a predetermined operation of the circuit consisting of shift registers 11-14, selectors 15-18 and exclusive OR circuit 20 (i.e., considered to correspond to the claimed "logic circuit"). Accordingly, unlike the claimed "arithmetic circuit," the arithmetic circuit 21 in the **AAPA** does not multiply predetermined initial values by a matrix produced by a predetermined operation of a logic circuit.

Further, it is believed that it is clear from Fig. 16 that the arithmetic circuit 21 shown in Fig. 16 multiplies the ***predetermined initial values Ri = Ri_3-Ri_0*** stored in initial value buffer 22 by ***matrices $M_{3(100)}$, $M_{2(100)}$, $M_{1(100)}$, $M_{0(100)}$*** that are stored in advance. It is also believed to be clear from the figure that the matrices $M_{3(100)}$, $M_{2(100)}$, $M_{1(100)}$, $M_{0(100)}$ are not matrices produced by the logic circuit. More specifically, as shown in Fig. 16, the arithmetic circuit 21 supplies matrices $R0_3$, $R0_2$, $R0_1$ and $R0_0$ to the logic circuit. However, any matrix or matrices produced by the logic circuit (i.e., elements 11-18) are not supplied to the arithmetic circuit 21.

Therefore, it is respectfully submitted that because the logic circuit (elements 11-18) does not produce a matrix or matrices that are supplied to the arithmetic circuit 21, the arithmetic circuit 21 cannot perform the operation of "multiplying said predetermined initial values stored in said storage circuit by said ***matrix produced by said logic circuit***", as recited in claims 16 and 20.

Accordingly, in view of the above amendments and remarks, it is respectfully submitted that claims 16 and 20 patentably distinguish over the cited prior art. Reconsideration and withdrawal of the rejection under §102 are respectfully requested.

CONCLUSION

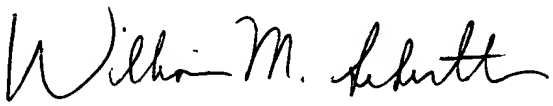
In view of the foregoing amendments and accompanying remarks, it is submitted that all pending claims are in condition for allowance. A prompt and favorable reconsideration of the rejection and an indication of allowability of all pending claims are earnestly solicited.

If the Examiner believes that there are issues remaining to be resolved in this application, the Examiner is invited to contact the undersigned attorney at the telephone number indicated below to arrange for an interview to expedite and complete prosecution of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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